

**UNITED STATES PATENT APPLICATION**

**OF**

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**FOR**

**IN-PLANE SWITCHING LIQUID CRYSTAL DISPLAY DEVICE  
AND METHOD FOR FABRICATING THE SAME**

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This application claims the benefit of Korean Patent Application No. 2000-39404, filed on July 10, 2000, which is hereby incorporated by reference as if fully set forth herein.

## **BACKGROUND OF THE INVENTION**

### **Field of the Invention**

The present invention relates to a liquid crystal display device, and more particularly to a liquid crystal display device implementing in-plane switching (IPS), where an electric field applied to liquid crystal is generated in a plane parallel to a substrate.

### **Discussion of the Related Art**

Recent liquid crystal display devices use the optical anisotropy and polarization properties of liquid crystal molecules to produce an image. Liquid crystal molecules have a definite orientational alignment as a result of their long, thin shapes. That orientational alignment can be controlled by an applied electric field. In other words, as an applied electric field changes, so does the alignment of the liquid crystal molecules. Due to the optical anisotropy, the refraction of incident light depends on the orientational alignment of the liquid crystal molecules. Thus, by properly controlling an applied electric field a desired light image can be produced.

While various types of liquid crystal display devices are known, active matrix LCDs (AM-LCDs) having thin film transistors and pixel electrodes arranged in a matrix are probably the most common. This is because such AM-LCDs can produce high quality images at reasonable cost.

Recently, light and thin liquid crystal display (LCD) devices with low power consumption are used in office automation equipment and video units and the like. Driving

methods for such LCDs typically include a twisted nematic (TN) mode and a super twisted nematic (STN) mode. Although TN-LCDs and STN-LCDs have been put to practical use, they have a drawback in that they have a very narrow viewing angle. In order to solve the problem of narrow viewing angle, in-plane switching liquid crystal display (IPS-LCD) devices have been proposed. The IPS-LCD devices typically include a lower substrate (often referred to as an array substrate) where a pixel electrode and a common electrode are disposed, an upper substrate having no electrode, and a liquid crystal interposed between the upper and lower substrates.

A detailed explanation for operation modes of a typical IPS-LCD device will be provided referring to FIGs. 1 to 5.

FIG. 1 is a cross-sectional view illustrating a typical IPS-LCD device. As shown in FIG. 1, lower and upper substrates 30 and 32 are spaced apart from each other, and a liquid crystal 10 is interposed therebetween. The lower and upper substrates are called array and color filter substrates, respectively. Pixel and common electrodes 34 and 36 are disposed on the lower substrate 30. The pixel and common electrodes 34 and 36 are parallel with and spaced apart from each other. Although not depicted in FIG. 1, a color filter is usually disposed on a surface of the upper substrate 32 and opposes the lower substrate 30. The pixel and common electrodes 34 and 36 apply an electric field 35 to the liquid crystal. The liquid crystal has a negative dielectric anisotropy, and thus it is aligned parallel with the electric field 35.

FIGs. 2 to 5 conceptually illustrate operation modes of a conventional IPS-LCD device. Referring to FIGs. 2 and 3, when there is no electric field between the pixel and the common electrodes 34 and 36, i.e., OFF state, the long axes of the liquid crystal molecules maintain an angle from a line perpendicular to the parallel pixel and common electrodes 34 and 36. Herein, the angle is 45 degrees, for example.

On the contrary, when the pixel and common electrodes 34 and 36 receive voltages, i.e., ON state, there is the in-plane electric field 35 parallel to the surface of the lower substrate 30 between the pixel and common electrodes 34 and 36, as shown in FIGs. 4 and 5. The in-plane electric field 35 is parallel to the surface of the lower substrate 30 because the pixel and common electrodes 34 and 36 are formed on the lower substrate 30. Accordingly, the liquid crystal molecules are twisted such that the long axes thereof are aligned with the direction of the electric field. Thus, the liquid crystal molecules are aligned such that the long axes thereof are parallel with the line perpendicular to the pixel and common electrodes 34 and 36.

By operating in the modes described above and with additional elements such as polarizers and alignment layers, the IPS-LCD device displays images. The IPS-LCD device has wide viewing angles and low color dispersion because the pixel and common electrodes are placed together on the lower substrate. These wide viewing angles of the IPS-LCD device are about 70 degrees in up-and-down and right-and-left sides. Moreover, the fabricating processes of this IPS-LCD device are simpler than other various LCD devices.

However, because the pixel and common electrodes are disposed on the same substrate (i.e., the lower substrate), the transmittance and aperture ratio are low. Further, there are some other disadvantages in the conventional IPS-LCD device. For example, the response time of the conventional IPS-LCDs is relatively slow and should be improved. In addition, the cell gap of the conventional IPS-LCDs provides very small margins for misalignment and should be improved to be more uniform.

For the sake of discussing the above-mentioned IPS-LCD device in detail, with reference to FIG. 6, the basic structure of the IPS-LCD device will be described in detail.

FIG. 6 is a plan view illustrating an array substrate of the conventional IPS-LCD device.

As shown, gate lines 50 and 51 and common line 54 are transversely arranged parallel with each other. Data lines 60 and 61 are arranged perpendicular to the gate and common lines 50 (and 51) and 54. Gate electrode 52 and source electrode 62 are positioned near a cross point of the gate and data lines 50 and 60, and communicate with the gate line 50 and the data line 60,  
5 respectively. Herein, the source electrode 62 overlaps a portion of the gate electrode 52.

A plurality of common electrodes 54a are positioned spaced apart from each other and perpendicular to the common line 54. The common electrodes 54a communicate with the common line 54. Some common electrodes 54a also communicate with a common electrode connector 54b that is parallel to the gate line 50 and positioned at first ends of the common electrodes 54a. A first pixel connecting line 66 communicates with a drain electrode 64, and a  
10 plurality of pixel electrodes 66a are positioned perpendicular to the first pixel connecting line 66. First ends of the pixel electrodes 66a communicate with the first pixel connecting line 66, and the second ends of pixel electrodes 66a communicate with a second pixel connecting line 68 that is positioned over the common line 54. Accordingly, the common electrodes 54a and the pixel  
15 electrodes 66a are parallel with and spaced apart from each other in an alternating pattern.

FIGs. 7A to 7D are cross-sectional views taken along the line VII-VII of FIG. 6 and illustrate steps of manufacturing processes of the array substrate for use in the conventional IPS-LCD device.

Referring to FIG. 7A, a first metal layer is deposited on a substrate 1 and then patterned  
20 to form the gate lines 50 and 51 (see FIG. 6), the gate electrode 52, the common line 54 (see FIG. 6) and the plurality of common electrodes 54a. Further, the common electrode connector 54b is also formed with the common electrodes 54a. Aluminum (Al), Chrome (Cr), Molybdenum (Mo) or Tungsten (W) is mainly used for the first metal layer.

Now, referring to FIG. 7B, a gate insulation layer 70 is deposited on the substrate 1 to cover the patterned first metal layer. Next, an active layer 72 is formed on the gate insulation layer 70, especially over the gate electrode 52. The gate insulation layer 70 is usually made of Silicon Nitride ( $\text{SiN}_x$ ) or Silicon Oxide ( $\text{SiO}_2$ ), while the active layer comprises a pure amorphous silicon (a-Si:H) and an impurity-doped amorphous silicon ( $n^+$  a-Si:H).

Referring to FIG. 7C, a second metal layer is deposited on the gate insulation layer 70 and active layer 72, and then patterned so as to form the source and drain electrodes 62 and 64, the data line 60 (and 61 of FIG. 6) and the plurality of pixel electrodes 66a. Further, the first and second pixel connecting lines 66 and 68 (see FIG. 6) are formed with the pixel electrodes 66a. Aluminum (Al), Chrome (Cr), Molybdenum (Mo) or Tungsten (W) is mainly used for the second metal layer, like the first metal layer.

As shown in FIG. 7C, the source and drain electrodes 62 and 64 are formed on the active layer 72 and particularly over portions of the gate electrode 52 such they respectively overlap opposite ends of the gate electrode 52. The pixel electrodes 66a are formed on the gate insulation layer 70 and spaced apart from each other. Also, each pixel electrode 66a is parallel with and spaced apart from the adjacent common electrodes 54a.

Referring to FIG. 7D, a passivation layer 74 is formed on the surfaces of the above-mentioned intermediates. The passivation layer 74 has a high humidity resistance and a high durability in order to protect the active layer 72 from being affected by moisture, foreign substances, etc.

As described above, the IPS-LCD device includes the common and pixel electrodes 54a and 66a in the array substrate such that the wide viewing angle can be achieved. However, the aperture ratio is poor because the common and pixel electrodes 54a and 66a are formed of the

opaque metal like the source and drain electrodes 62 and 64.

Further, referring back to FIG. 6, an area "A" between the data line 60 and the adjacent common electrode 54a, an area "B" between the data line 61 and the adjacent common electrode 54a, and an area "C" between the common line 54 and the adjacent gate line 51 are non-display areas. Namely, these areas "A", "B" and "C" do not affect image display because the liquid crystal in these areas does not properly function and is not operated when the voltage is supplied to the plurality of pixel electrodes 66a. Therefore, a black matrix covers these areas "A", "B" and "C" in a later manufacturing step. As a result, the black matrix shields these areas "A", "B" and "C" from light generated from the backlight device (not show), thereby diminishing the brightness of the IPS-LCD device. Furthermore, in order to prevent the short circuit between the gate line 51 and the common line 54 when forming the gate and common lines 51 and 54 in the same plane, the area "C" is enlarged, thereby resulting in lowering the aperture ratio.

Still referring to FIG. 6, the common electrodes 54a adjacent to the data lines 60 and 61 are affected by the cross talk when the data lines 60 and 61 receive the signal voltages. Thus, the common electrodes 54a need to be far away from the data lines 60 and 61, and the areas "A" and "B" are enlarged to decrease this cross talk. Therefore, the aperture ratio is accordingly decreased.

As widely known, the aperture ratio is closely related to the brightness. Further, the stronger the brightness is, the more powerful the backlight device is. From these reasons, the above-mentioned IPS-LCD device has high power consumption.

### **SUMMARY OF THE INVENTION**

Accordingly, the present invention is directed to an IPS-LCD device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide an IPS-LCD device having a high aperture ratio.

Another object of the present invention is to provide the IPS-LCD device that has a high brightness.

5 Additional features and advantages of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

10 In order to achieve the above object, the preferred embodiment of the present invention provides an in-plane switching liquid crystal display (IPS-LCD) device including first and second substrates opposite to and spaced apart from each other; a gate line arranged in one direction on the first substrate; a common line arranged on the first substrate, the common line being parallel with the gate line and spaced apart from the gate line; a gate insulation layer on the substrate, the gate insulation layer covering the common and gate lines; a data line on the gate insulation layer, the data line being perpendicular to the gate line; a thin film transistor receiving signals from the gate and data lines, the thin film transistor including a gate electrode, the gate insulation layer, an active layer, and source and drain electrodes; a first passivation layer on the gate insulation layer so as to cover the thin film transistor and data line, the first passivation layer having a plurality of common line contact holes that penetrate both the first passivation layer and the gate insulation layer to the common line so as to expose portions of the common line; a plurality of common electrodes being parallel with the data line on the first passivation layer, each common electrode contacting the common line through each common line contact hole; a second

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passivation layer on the first passivation layer so as to cover the plurality of common electrodes, the second passivation layer having a drain contact hole that penetrates both the first and second passivation layer to the drain electrode of the thin film transistor; a pixel connecting line being parallel with the gate line on the second passivation layer, the pixel connecting line contacting the drain electrode through the drain contact hole; a plurality of pixel electrodes perpendicularly extending from the pixel connecting line, each pixel electrode arranged between the adjacent common electrodes; and a liquid crystal layer between the first and second substrates.

The common and pixel electrodes and the pixel connecting line are formed of the transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO).

The gate insulation layer and the second passivation layer are one of Silicon Nitride ( $\text{SiN}_x$ ) and Silicon Oxide ( $\text{SiO}_2$ ).

The first passivation layer is formed of an organic material such as benzocyclobutene (BCB) or acryl.

In order to accomplish the above objects, the principles of the present invention further provide a method of fabricating an array substrate for use in an in-plane switching LCD device, including: forming a gate electrode, a gate line and a common electrode on a substrate by depositing and then patterning a first metal layer; forming a gate insulation layer on the substrate to cover the patterned first metal layer; forming an active layer on the gate insulation layer and over the gate electrode; forming a data line and source and drain electrodes by depositing and then patterning a second metal layer, the data line being perpendicular to the gate line on the gate insulation layer, the source electrode extending from the data line over the active layer, and the drain electrode being spaced apart from the source electrode on the active layer; forming a first passivation layer on the gate insulation layer so as to cover the patterned second metal layer, the

first passivation layer having a plurality of common line contact holes that penetrate both the first passivation and gate insulation layers to the common line; forming a plurality of common electrodes that are parallel with the data line on the first passivation layer, each common electrode contacting the common line through each common line contact hole; forming a second  
5 passivation layer on the first passivation layer so as to cover the plurality of common electrodes, the second passivation layer having a drain contact hole that penetrates both the first and second passivation layer to the drain electrode; and forming a pixel connecting line and a plurality of pixel electrodes, the pixel connecting line being parallel with the gate line on the second passivation layer and contacting the drain electrode through the drain contact hole, the plurality  
10 of pixel electrodes perpendicularly extending from the pixel connecting line, and each pixel electrode arranged between the adjacent common electrodes.

A method of forming the plurality of common electrodes includes depositing and patterning a first transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO).

15 A method of forming the pixel connecting line and pixel electrodes includes depositing and patterning a second transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO).

The first passivation layer is an organic material such as benzocyclobutene (BCB) or acryl.

20 The gate insulation layer and the second passivation layer are one of Silicon Nitride ( $\text{SiN}_x$ ) and Silicon Oxide ( $\text{SiO}_2$ ).

First and second metal layers include a material selected from a group consisting of chromium (Cr), aluminum (Al), aluminum alloy (Al alloy), molybdenum (Mo), tantalum (Ta),

tungsten (W), antimony (Sb), and an alloy thereof.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

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### **BRIEF DESCRIPTION OF THE DRAWING**

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiment of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

FIG. 1 is a cross-sectional view illustrating a typical IPS-LCD device;

FIGs. 2 to 5 are perspective views conceptually illustrating operation modes of a conventional IPS-LCD device;

FIG. 6 is a plan view illustrating an array substrate of the conventional IPS-LCD device;

FIGs. 7A to 7D are cross-sectional views taken along the line VII-VII of FIG. 6 and illustrate steps of manufacturing processes of the array substrate for use in the conventional IPS-LCD device;

FIG. 8 is a plan view illustrating an array substrate of an IPS-LCD device according to the present invention; and

FIGs. 9A to 9E and 10A to 10D are cross-sectional views respectively taken along the lines IX-IX and X-X of FIG. 8 and illustrate steps of manufacturing processes of the array substrate for use in the IPS-LCD device according to the present invention.

**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Reference will now be made in detail to the preferred embodiment of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

FIG. 8 is a plan view illustrating an array substrate of an IPS-LCD device according to the present invention.

As shown in FIG. 8, a gate line 100 is transversely disposed on a substrate 1 (see FIG. 9A). A common line 120 is spaced apart from and is parallel to the gate line 100. Data lines 200 and 201 are spaced apart from each other and are disposed across and perpendicular to the gate and the common lines 100 and 120.

Near an intersection of the gate and data lines 100 and 200, gate and source electrodes 110 and 210 are positioned and electrically connected with the gate and data lines 100 and 200, respectively. A drain electrode 220, including a drain contact hole 240, is spaced apart from the source electrode 210 and overlaps a portion of the gate electrode 110. The source electrode 210 also overlaps a portion of the gate electrode 110.

A pixel connecting line 310 electrically contacts the drain electrode 220 through the drain contact hole 240, and is disposed parallel with the gate line 100. A plurality of pixel electrodes 300 are disposed perpendicular to the pixel connecting line 310, and communicate with the pixel connecting line 310.

A plurality of common electrodes 130 are disposed parallel with the pixel electrodes 300. Each common electrode 130a, 130b, 130c or 130d electrically contacts the common line 120 through a respective common line contact hole 131, and is spaced apart from the adjacent pixel

electrodes 300. Therefore, the common electrodes 130 are electrically connected to each other via the common line 120. As shown in FIG. 8, the common and pixel electrodes 130 and 300 are arranged in an alternating pattern.

The common line 120 and the gate and data lines 100 and 200 (and 201) are an opaque metal, while the common and pixel electrodes 130 and 300 are a transparent conductive material. Preferably, the opaque metal is selected from a group consisting of Chromium (Cr), Aluminum (Al), Aluminum alloy (Al alloy), Molybdenum (Mo), Tantalum (Ta), Tungsten (W), Antimony (Sb), and the like, while the transparent conductive material is Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO).

Now, referring to FIGs. 9A to 9E and 10A to 10D, a fabricating process for the array substrate shown in FIG. 8 is provided.

FIGs. 9A to 9E and 10A to 10D are cross-sectional views taken along the lines IX-IX and X-X of FIG. 8, respectively, and illustrate steps of the manufacturing process of the array substrate for use in the IPS-LCD device according to the present invention.

Referring to FIGs. 9A and 10A, a first metal layer is deposited on a substrate 1 and then patterned so as to form the gate line 100 (see FIG. 8), the gate electrode 110 and the common line 120. The gate electrode 110 is extended from the gate line 100 of FIG. 8. As mentioned before, Chromium (Cr), Aluminum (Al), Aluminum alloy (Al alloy), Molybdenum (Mo), Tantalum (Ta), Tungsten (W), Antimony (Sb), or the like is used for the first metal layer.

Thereafter, a gate insulation layer 132 is deposited on the substrate 1 to cover the patterned first metal layer. Next, an active layer 134 is formed on the gate insulation layer 132, especially over the gate electrode 110. The gate insulation layer 132 is usually made of Silicon Nitride ( $\text{SiN}_x$ ) or Silicon Oxide ( $\text{SiO}_2$ ). The active layer 134 is comprised of a pure amorphous

silicon (a-Si:H) 134a and an impurity-doped amorphous silicon ( $n^+$  a-Si:H) 134b.

Now, referring to FIGs. 9B and 10B, a second metal layer is deposited on the gate insulation layer 132 and active layer 134, and then patterned so as to form the source and drain electrodes 210 and 220 and the data lines 200 and 201. The source electrode 210 is extended from the data line 200 and the drain electrode 220 is spaced apart from the source electrode 210. Both source and drain electrodes 200 and 220 overlap the opposite ends of the gate electrode 110. After forming the source and drain electrodes 210 and 220, a portion of the impurity-doped amorphous silicon 134b between the source and drain electrodes 210 and 220 is removed in order to form a channel region "CH" on the pure amorphous silicon 134a. Accordingly, a thin film transistor (TFT) "S" is complete. The source and drain electrodes 210 and 220 and the data lines 200 and 201 are usually made of the same material as the first metal layer.

Referring to FIGs. 9C and 10C, a first passivation layer 136 is formed on the surfaces of the above-mentioned intermediates, so the first passivation layer 136 covers the TFT "S" and the patterned second metal layer. For a first passivation layer 136, an organic material such as benzocyclobutene (BCB) or acryl is used due to its superior light transmittance and low dielectric constant. Thereafter, the common line contact holes 131 are formed over the common line 120, as shown in FIG. 10C. The common line contact holes 131 penetrate both the first passivation layer 136 and the gate insulation layer 132 in order to expose the portions of the common line 120.

Still referring to FIGs. 9C and 10C, a first transparent conductive material is deposited on the first passivation layer 136 and then patterned to form a plurality of common electrodes 130 that are bar-shaped, as shown in FIG. 8. As aforementioned, the first transparent conductive material is Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO). Each common electrode 130a,

130b, 130c or 130d is parallel with the data lines 200 and 201, and spaced apart from each other. Further, the common electrodes 130 contact the common line 120 through the common line contact holes 131.

Now, referring to FIGs. 9D and 10D, a second passivation layer 137 is deposited on the first passivation layer 136 to cover the common electrodes 130. The second passivation layer 137 is preferably silicon nitride ( $\text{SiN}_x$ ) or silicon oxide ( $\text{SiO}_2$ ). Thereafter, the drain contact hole 240 is formed by patterning the portion of both the first and second passivation layers 136 and 137. Namely, the drain contact hole 240 penetrates the first and second passivation layers 136 and 137 and exposes the portion of the drain electrode 220 of the TFT "S".

Referring to FIG. 9E, a second transparent conductive material is deposited on the second passivation layer 137 having the drain contact hole 240. Thereafter, the second transparent conductive material is patterned so as to form the pixel electrodes 300 and pixel connecting line 310. Since the pixel electrodes 300 are connected with the pixel connecting line 310, which contacts the drain electrode 220 through the drain contact hole 240, the pixel electrodes 300 electrically communicates with the drain electrode 220. Each pixel electrode 300 is arranged between the adjacent common electrodes, such that pixel and the common electrodes are disposed in an alternating manner as shown in FIGs. 8 and 9E. Here, the second transparent conductive material is Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO), like the first transparent conductive material.

As described hereinbefore, the array substrate according to the present invention includes three insulating layers (i.e., the gate insulation layer and the first and second passivation layers). Each insulating layer insulates the conductive layers (i.e., the patterned first and second metal layer and the patterned first and second transparent conductive material) against each other.

Since the organic material is used for insulating the data line against the common electrodes, areas between the data line and the common electrodes (see reference letters "A" and "B" of FIG. 6) can be reduced. Namely, the organic material such as benzocyclobutene (BCB) or acryl has a low dielectric constant, and thus, cross talk between the data line and the common electrode is substantially minimized. For example, the data line 201 is insulated against the common electrode 130d as shown in FIG. 9E. Thus, the area between the data line 201 and the common electrode 130d can be reduced. Therefore, the common electrode can be closer to the data line, thereby raising the aperture ratio. As a related advantage, the brightness of the IPS-LCD device increases according to the present invention.

Furthermore, compared to the conventional IPS-LCD device, the array substrate of the inventive IPS-LCD device has the common line and common electrodes in different planes. Namely, the common electrodes are not formed when forming the common line. As described before, the common electrodes are formed on the first passivation layer, i.e., the organic material, and contact the common line through the common line contact holes that penetrate both the passivation layer and the gate insulation layer. Moreover, the common electrodes are formed of the transparent conductive material such as ITO or IZO. Further, the pixel electrodes and the pixel connecting line are also made of this transparent conductive material. The transparent conductive material is substantially substituted for the opaque metal in the present invention, compared to the conventional art. As a result, the brightness of the IPS-LCD device also increases according to the present invention. As a related advantage, the overall brightness of the backlight device can be lowered because more light passes through the IPS-LCD, and thus, low electric power consumption can be obtained. Compared with the aperture ratio of a conventional IPS-LCD device employing the opaque metal as the common and pixel electrodes, the aperture



ratio of the inventive IPS-LCD device employing the array substrate with the transparent common and pixel electrodes increases by more than 10 %. Therefore, the aperture ratio problem of the conventional IPS-LCD device is reduced or eliminated.

As described herein, the IPS-LCD device according to the preferred embodiments of the present invention has the following advantages.

First, because of the transparent common and pixel electrodes, the aperture ratio is increased.

Second, because of the high aperture ratio, the light generated from the backlight device largely passes through the substrates, thereby improving the brightness of the IPS-LCD device.

Third, because of the improved brightness, the electric power consumption of the backlight device is decreased.

Fourth, due to the organic material that insulates the data lines against the common electrodes, the cross talk that is created by the signals flowing the data lines and affects the common electrodes is minimized, thereby allowing a reduced distance between the data lines and the common electrodes. Therefore, the aperture ratio increases as well.

It will be apparent to those skilled in the art that various modifications and variation can be made in the array substrate and the manufacturing method thereof of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.